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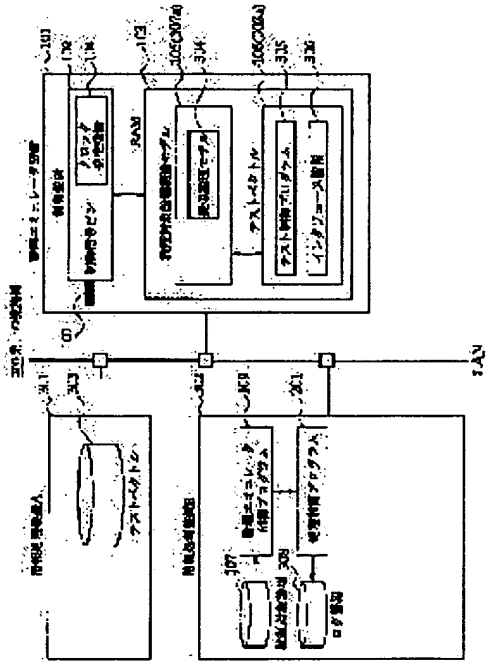
(54) LOGIC VERIFYING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To perform fast and efficient logic verification which is superior in operability and observing performance.
SOLUTION: A dummy logic model 304 providing the I/O environment, etc., of a logic structure model 105 to be verified is built in the logic model 105 mounted on a logic emulator device 101, a test control program 305 which controls logic verifying operation by input to the logic structure model 105 of a test vector 303a is built in the test vector 303a, and test information is sent and received between the dummy logic model 304 and test control program 305 from a process control program 201 having a GUI interface described in an external general language through interface information 306 to improve the operability and observing performance of logic verification by the GUI interface, thereby achieving the consistent logic verification of a lage-scale logic device by the fast logic emulator device 101.



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CLAIMS

[Claim(s)]
[Claim 1] In the test vector used for the logic verification in the exclusive testing device with which the real chip of the logic emulator with which the logical structure model of the purpose logical unit for verification was mounted, or said purpose logical unit was mounted In delivering and receiving information between the processing control programs formed in the exterior of said logic emulator or said exclusive testing device The logic verification approach characterized by mounting the test control program which makes controllable said logic verification by the input of said test vector from said processing control program.
[Claim 2] In the logic verification approach according to claim 1 in said logic emulator The 1st logical structure model for realizing said purpose logical unit and an identification logical function, The 2nd logical structure model for realizing a part of logical function [at least] which offers the operating environment of said 1st logical structure model is mounted. The logic verification approach characterized by performing logic verification of said purpose logical unit, without needing connection with the external hardware for realizing the execution environment of said purpose logical unit.
[Claim 3] In the logic verification approach according to claim 1 or 2 said processing control program The function which delivers and receives information between said test control programs, the function which deliver and receive information between the logic emulator control programs which control said logic emulator, The function which delivers and receives information between the logic simulators who perform logic verification of said purpose logical unit by software, The function which delivers and receives information between said exclusive testing devices, said test control program, Said logic emulator control program, said logic simulator, the general-purpose graphical user interface that performs registration of visualization presenting of said information, or a user input delivered and received between at least one of said the exclusive testing devices, ** -- the logic verification approach characterized by having at least one.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] About logic verification technique, especially this invention is applied to a logic simulator, the functional verification technique of the logical circuit equipment using a logic emulator, etc., and relates to an effective technique.
[0002]
[Description of the Prior Art] The logic emulation using conventional logic emulation equipment (logic emulator) carried out logic compile of the logical structure model which described actuation with the behavioral description language and was designed in the logical model which are a system unit for logic verification, and some logical chips, and mounted it in RAM in logic emulation equipment, and the in circuit method which emulates logical-model actuation was performing logic verification. Moreover, equipment and the logical chip which are not an in circuit connected the mutual external signal line to the external contact pin of logic emulation equipment, in order to secure an interface with in circuit logic, and they have taken the synchronization of operation on signal value level. Moreover, when observation and the test vector of logic actuation were specified according to an individual, to the internal signal which can be observed and external pin in logic emulation equipment, the logical value was given, or observation in a signal-line unit was performed to the signal line specified beforehand, and logic actuation was checked.
[0003] About such a logic emulation technique, the approach as shown in JP,02-245831,A etc. is learned. That is, by mapping the logical function for verification on a programmable gate array from the outside, the logical function of the purpose tends to be realized in hardware and it is going to enable high-speed activation and logic verification.
[0004]
[Problem(s) to be Solved by the Invention] It cannot say that the conventional in circuit method is enough to secure logic quality like systems testing to increase of a logic scale in recent years, or the complexity of logic for the logic emulation in partial logic, but the system-logic verification by the logic emulation in the whole logical chip is needed. In order to have to set a logical value as all signal lines in the logic emulation which increase of a logic scale and complication of logic also progress, and gives the logical value in the conventional signal-line level, or observes the value of a signal line in logic verification with the whole logical chip, it is difficult to perform efficient logic verification. In order to raise observation nature and operability, it is necessary to enrich a man machine interface and to raise test ease.
[0005] Moreover, a logic simulator takes time amount immense to logic verification to the logic simulation in the whole logical chip compared with hardware actuation for software actuation in order to create a logical model by software, it carries out short-term development of the product, and application is difficult and is one of the technical problems which must be solved by the end of today when early shipment must be carried out.
[0006] Moreover, it is necessary to use together the architecture logic simulator by which logic for verification may be unable to check logic verification actuation with a logic simple substance in the case of the logic of a peripheral device etc., and verification level differs, and to perform

logic verification, and using the logic simulator of dedication. [performing logic verification of the logic for verification] Therefore, construction of the logic emulation method which chooses an efficient logic simulator and can be used together on systems testing level is an important technical problem.

[0007] Moreover, when a real chip is manufactured in the phase which the logic emulation ended and logic quality inspection in a chip simple substance or the whole equipment is carried out, when the logic verification environment till then could be continued and used and poor logic is discovered, feedback to a logic simulation or a logic emulation is easy, and the logic verification environment which having considered construction of a verification environment was consistent needs to be built.

[0008] The purpose of this invention is to offer the logic verification technique which can perform efficiently system-logic verification by the logic emulation in the whole logical chip for a short time.

[0009] Other purposes of this invention enrich a man machine interface, and are to offer the observation nature of the internal state in a logic emulation, operability, and the logic verification technique that can raise test ease further.

[0010] Other purposes of this invention are to offer the logic verification technique which can realize logic verification which cohered until it resulted [from a logical model] in a real chip.

[0011] Other purposes of this invention are to offer the logic verification technique which the man day and period which environmental construction of logic verification takes are shortened, and can realize the cost reduction in a logic verification process.

[0012]

[Means for Solving the Problem] This invention mounts the false logical model which offers the execution environment of the logical structure model concerned in operating with the logical structure model and logical structure model of the purpose logical unit on a logic emulator for the purpose of logic verification of the purpose logical unit, and mounts the test control program which controls logic verification actuation by delivering and receiving information between external processing control programs in the test vector performed on a logic emulator.

[0013] A false logical model, a program, and the processing control program that controls a logic emulator For example, a means for it to be mounted on the information processor connected to the logic emulator through the network, and to perform an information communication link between a logic emulator and the processing control program concerned, A means to operate a logic emulator to asynchronous, and the graphical user interface which offers visualization presenting of various information, an informational input environment, etc., The connecting plug interface which connects to the processing control program concerned the logic verification program from which the verification technique, such as logic simulators other than a logic emulator, differs, It has the interface with the test control program and test vector which operate on a logic emulator, and the operability and observation nature of logic verification of the purpose logical unit are raised, and logic verification is enabled efficiently at a high speed.

[0014] Moreover, in the exclusive testing device with which the real chip of the purpose logical unit is mounted, the test control program which controls logic verification actuation by delivering and receiving information between external processing control programs is mounted in the test vector inputted into a real chip. In this case, a processing control program is mounted in the information processor to which the exclusive testing device other than an above-mentioned configuration is connected through the connection interface of arbitration, has the driver control program which delivers and receives information on the device driver which controls said connection interface, raises the operability and observation nature in logic verification of a real chip, and performs logic verification at a high speed efficiently. Moreover, the case of a logic emulator and a common thing can be used for a test vector, and a test control program and a processing control program.

[0015] Moreover, in a processing control program with the interface of the test control program in a test vector, and a false logical model, the observation and control of the logical model of the purpose logical unit of an internal signal value which were mounted in the logic emulator are performed, and logic verification of the purpose logical unit can be performed, controlling a

processing state as an I/O request and controlling a logic emulator by a processing control program transmitting and receiving a test control program and an I/O request.
[0016]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail, referring to a drawing.
[0017] Drawing 1 is the conceptual diagram showing an example of the configuration of the information processing system with which the logic verification approach which is the gestalt of operation of the first of this invention is enforced, and drawing 2 is the conceptual diagram which illustrated an example of the configuration of the software for realizing the logic verification approach of this invention. Moreover, drawing 8 is the conceptual diagram showing an example of the logic emulation structure of a system of the reference technique of the logic verification approach of the gestalt of this operation.
[0018] First, the outline of the logic emulation system of the reference technique of the gestalt of this operation is explained before explanation of the gestalt of this operation using drawing 8 .
[0019] The logic emulation system 100 of drawing 8 consists of logic emulator control programs 109 which operate on the logic emulator equipment 101 by which LAN connection was made, and the information processor 108 by which LAN connection was similarly made. Logic emulator equipment 101 consists of RAM103 in which a control unit 102 and R/W are possible, and consists of clock generation equipment 104 which makes a control unit 102 generate the clock of operation supplied to logic emulator equipment 101, a control signal pin 107 for logic emulation control, etc. In addition, only the component about this invention is explained by specializing.
[0020] The control signal pin 107 is an external pin for reporting an emulation condition to the logic emulator control program 109, or receiving directions of operation. Since the below-mentioned logical structure model 114for verification a is mounted in the logical structure model storage area 105 for verification or a test vector is mounted in the test vector storage area 106, RAM103 is used. The logic emulator control program 109 consists of the control section 110 for controlling logic emulator equipment 101 and the logic emulator control program 109, the RAM access section 112, a logic compiler 111 that carries out logic compile of the logic 114 for verification described with the behavioral description language, and a graphical user interface (GUI) control section 113 which displays and controls the whole logic emulation system graphically. The logic compiler 111 considers logic 114 for verification as an input, carries out logic compile and mounts it in the logical structure model storage area 105 for verification of RAM103 in logic emulator equipment 101 as logical structure model 114for verification a.
[0021] Next, the procedure of actually performing a logic emulation is explained. After carrying out logic compile of the logic 114 for verification mentioned above, being referred to as logical structure model 114for verification a and mounting in RAM103, a test vector is mounted in the test vector storage area 106 by the RAM access section 112, by the control section 110, operating-condition information is actually supplied to a clock by delivery and clock generation equipment 104 to the control signal pin 107, logic emulator equipment 101 is operated, and a logic emulation is performed. Next, emulation operating state information is set to the control signal pin 107, a control section 110 supervises this information, after performing a fixed cycle logic emulation, according to that status information, a clock is supplied succeedingly, or it is interrupted and a control unit 102 observes the condition of RAM103. Logic verification is performed by repeating these processings and performing them.
[0022] Next, an example of the processing control program for realizing the logic verification approach of the gestalt each operation of this invention to drawing 2 is shown. The interprocess communication control section 203 which performs interprocess communication between the logic emulator control programs 109 with which the processing control program 201 was started on the network, The logic emulator control section 204 and the test vector control section 205, The data-conversion section 206 which performs transform processing of the data transmitted and received between logic emulator equipment 101, The connecting plug interface 207 for connecting the verification equipment and the verification systems other than logic emulator equipment 101 to the processing control program 201, the graphical user interface (GUI) control section 202 which controls the logic verification method of this invention synthetically -- it is

come out and constituted. In addition, explanation of each detailed processing section is given by explanation of the gestalt of operation. Moreover, although the configuration containing all the components of the interprocess communication control section 203 - the connecting plug interface 207 is illustrated by it since it is easy for drawing 2 , the configuration only containing the required component of these is also included in this invention.

[0023] Next, the logic emulation system by which the logic verification approach which is the gestalt of operation of the first of this invention is enforced using drawing 1 is explained. In the logic emulation system 300 of the gestalt of the first operation shown in drawing 1 , logic compile of the logic for verification is carried out as logic which realized functional level architecture, it sets to RAM103 of logic emulator equipment 101, and the technique of performing logic verification is explained.

[0024] in addition, in the logic emulation system 300 of the gestalt of this operation Logic emulator equipment 101 is set to logic verification of an in circuit method. By mounting the below-mentioned false logical model 304 in logic emulator equipment 101 Vector verification in the condition of having mounted only the logical structure model for verification is enabled, and in order to offer the actual operating environment of the logical model for verification (real chip which performs identification actuation), it is not necessary to connect surrounding hardware circuitry to logic emulator equipment 101.

[0025] For example, when the candidate for verification is a microprocessor, in the logic emulation system 100 of a reference technique which was illustrated by drawing 8 since it was necessary to realize an I/O environment with the circumference circuit use for construction of an actual system, the hardware environment of a circumference circuit is beforehand prepare for verification of the logical function of the whole, and it is necessary to make wiring connection to the logic emulator equipment 101 which emulates actuation of a microprocessor. On the other hand, since the below-mentioned false logical model 304 realizes an I/O interface required for actuation of logical structure model 307for verification a of the purpose in the case of the logic emulation system 300 of the gestalt of this operation, the connection (in circuit connection) to an actual circumference circuit etc. is unnecessary, and verification actuation is [the simple substance of logic emulator equipment 101] possible for it.

[0026] The test vector 303 is stored in the information processor 301 (A) connected to LAN with the gestalt of this operation. Moreover, the logic emulator control program 109 and the processing control program 201 are mounted and performed by the information processor 302 (B) connected to LAN. An information processor 301 (A) and an information processor 302 (B) consist of workstations, personal computers, etc. which operate by OS's, such as UNIX.

[0027] First, the logic 307 for verification and a test vector 303 are prepared as pre-preparation. The false logical model 304 which has an interface function with the processing control program 201 is built into the aforementioned logic 307 for verification, logic compile is carried out with the logic compiler 111, and it is referred to as logical structure model 307for verification a. It has the interface function of the function which observes or supervises the logical value of the internal signal line under logic actuation as a function of the false logical model 304, the system-control function to control actuation of the logic 307 (logical structure model 307for verification a) for verification, and the processing control program 201. Moreover, the interface information 306 used for the interface of the test control program 305 with an interface function with the processing control program 201 and the processing control program 201 is included in the test vector 303.

[0028] Next, the logic emulator control program 109 is started and the compile result of the prepared logic 307 for verification is set to the logical structure model storage area 105 for verification in RAM103 as logical structure model 307for verification a using the RAM access section 112.

[0029] Next, the processing control program 201 is started, and the prepared test vector 303 is changed into test vector 303a of the format which can be set to RAM103 in the data-conversion section 206, and it sets to the test vector storage area 106 in RAM103 by the RAM access section 210 course in the logic emulator control section 204.

[0030] A different point from the logic emulation system 100 of the reference technique shown

in drawing 8 is that the false logical model 304, the test control program 305 in test vector 303a, the interface information 306, and the processing control program 201 independent of the logic emulator control program 109 are formed.
[0031] Moreover, by creating the processing control program 201 by Tcl/Tk, since it has a Tcl/Tk interface, it is easily connectable [the logic emulator control program 109 of the gestalt of this operation] as part of the extension of the logic emulator control program 109 while being able to use the function of the logic emulator control program 109 of drawing 8 which is a reference technique as it is. That is, the processing control program 201 can be said to be the extended program which makes logic emulator equipment 101 operational from the outside.
[0032] in addition, the general-purpose script language which has with Tcl/Tk the graphical interface (GUI) developed in University of California at Berkeley -- it is -- as an opening shell script -- size besides many universities or a lab -- it is used in various companies.
[0033] Moreover, the Tcl/Tk interface adopted by this invention is because the logic emulator equipment of this example had the Tcl/Tk interface, and in case this invention is carried out, the GUI function to offer a man machine interface can be realized by the X Window System, Motif, etc. Furthermore, if it is the system which in other words had a GUI interface, the function or system will not be limited.
[0034] Next, it explains along with the procedure of actually performing a logic emulation. After test vector 303a is set, the setting information control section 215 performs various setup required for logic emulation actuation, such as a setup of detailed logic emulation actuation, a setup to the test control program 305, a detail setup of the interface information 306, and clock frequency. These setup is controlled by the GUI control section 113 or the GUI control section 202. After various setup is completed, the control section 209 of operation in the logic emulator control section 204 advances a reset demand to the false logical model 304, and changes the condition of logical structure model 307for verification a into the condition that it can operate. Then, the number of clocks of operation is given to the control signal pin 107, with clock generation equipment 104, only several specified clock minutes, a clock is supplied to logic emulator equipment 101, and a control unit 102 actually operates. While operating only several specified fixed clock minutes, the test control program 305 sets an interior-action condition, test operating state, etc. to the interface information 306. Moreover, when an emulation is interrupted or output requests, such as a message, occur with the test control program 305 to the processing control program 201, without reaching the specified number of clocks, the status information is set to the interface information 306.
[0035] Since the false logical model 304 is supervising the interface information 306, if these demands are detected, to the control signal pin 107 of a control device 102, it will generate a trigger event and will perform an interruption report to a control device 102. Thus, the false logical model 304 has the function to interrupt emulation actuation, and an informational exchange is possible for it at the processing control program 201 and the direct interactive mode. That is, an emulation can be interrupted for supervising the value of the internal signal inside logic, and the information can be transmitted to the processing control program 201 by it.
[0036] Next, the interface information 306 in which interruption information is stored if a trigger event is detected, since the trigger event control section 208 of the processing control program 201 is supervising the control signal pin 107 is acquired by RAM access section 210 course, and the acquired information is changed in the data-conversion section 206, in order to display, and it displays by handing over to a display 212. When acquisition information is analyzed by the test vector control section 205 and the test control program 305 is demanding the input or the command from interruption information, by the input-control section 213, an operator's key input and GUI window operation are received, and the inputted information is set to the interface information 306. After setting, a logic emulation will be continued if a clock is supplied.
[0037] In addition, when saving these emulation results and working conditions, by the log data extraction control section 216, the displayed information, the inputted information, accessible RAM information, etc. can be acquired, and it can save as log information 308. Moreover, the processing control section 211 and the window control section 214 control the processing control program 201 consistently, and support various actuation.

[0038] It becomes possible to secure a dialogue means with the false logical model 304 of dedication in logic emulator equipment 101 by performing a logic emulation to the test control program 305 in RAM103, and a dialogue using the various functions of the GUI control section 202, and the test vector control section 205 as mentioned above, and in logic emulation actuation, control of a logic emulation is possible at actuation of only the interface information 306, and efficient logic verification is [operability and observation nature are raised and] possible. Moreover, since such technique is controlling the logic emulator control program 109 indirectly, it includes the reference technique illustrated by drawing 8 , and is controllable in logic emulator equipment 101 from the outside on it. Furthermore, since it makes to interrupt a logic emulation since logic emulation actuation is controllable with the test control program 305 into the minimum and can make the most of the rapidity of logic emulator equipment 101, a high-speed logic emulation is possible.
[0039] Next, an example of the concrete processing flow in the logic emulation of the gestalt of the first operation is shown in drawing 3 . Drawing 3 explains the processing flow only about an operation of the component of the gestalt of this operation when the test control program 305 in the middle of logic emulation actuation generates a message output demand and a command input demand. First, the processing stage in drawing 3 is classified into the stage of an operator 401, the processing control program 201, the false logical model 304, and the test control program 305, and shows cooperation actuation of each [these] stage as a processing flow.
[0040] If the above-mentioned logic 307 for verification and an above-mentioned test vector 303 are set to RAM103 as logical structure model 307for verification a, and test vector 303a, respectively and a clock is supplied to them, when they will be in the condition which can start an emulation, an operator performs initiation directions of operation (step 402). The number of clocks of operation (the number of operating cycles) is directed in initiation directions of this step 402 of operation. Next, the processing control program 201 actually performs emulation initiation (step 403), and logic emulator equipment 101 starts a logic emulation. If a logic emulation is started, the false logical model 304 and the test control program 305 will start actuation (step 404). At this time, the false logical model 304 is always supervising interface information 306 (step 405). And in order that the test control program 305 may report a message to an operator working, when a message output demand occurs and the input request of a response command to the message occurs further (step 406), the test control program 305 sets to the interface information 306 the event information that an outgoing message and the false logical model 304 are detectable (step 407). Next, the false logical model 304 detects an event by the monitor of the interface information 306 (step 408), and generates a trigger event to the control signal pin 107 (step 409). If a trigger event occurs, a control unit 102 will interrupt an emulation (step 410), and the processing control program 201 recognizes that it is interruption by the trigger event from a suspended state (step 411), and acquires the interface information 306 by RAM read-out (step 412). Data conversion of the acquired information is carried out through the data-conversion section 206 (step 413), and it is displayed on the window of a display 212 as an outgoing message from the test control program 305 (step 414). Usually, if it is only the output of a message, the emulation after a display will be resumed, but since the input command demand is also generated at coincidence in the case of the gestalt of this operation, the input request of a command is performed to an operator 401 (step 415), and the processing control program 201 will be in the state waiting for an input (step 417). An operator 401 keys (step 416) and inputs the command to the test control program 305. Next, the command which it keyed is acquired (step 418), data conversion is performed in the data-conversion section 206 (step 413), and RAM writing is performed that it should set to the interface information 306 (step 419). Next, emulation actuation is resumed (step 420) and the false logical model 304 and the test control program 305 resume actuation (step 421). After a restart acquires an input command from the interface information 306 (step 422), and actuation doubled with the command is performed (step 423).
[0041] Thus, interface information is mutually transmitted between an operator 401 and the test control program 305, an operator controls logic emulator equipment 101 by performing a logic emulation interactively from the exterior, and efficient logic verification is possible for the test

control program 305 by controlling logic emulator equipment 101 from the interior. In addition, since it is especially a logical model, it excels in observation nature, such as an internal signal, and in hardware, the false logical model 304 of the test control program 305 is controllable in logic emulator equipment 101 by software, and an efficient logic emulation is possible [the false logical model 304 which supervises the interface information 306 like the test control program 305 is also controllable from the interior in logic emulator equipment 101, and] for it.

[0042] That is, according to the gestalt of this operation, it is possible to perform system-logic verification by the logic emulation at a high speed efficiently the test control program 305 formed in test vector 303a of the test vector storage area 106, and by securing an interface with test vector 303a with the false logical model 304, and the processing control program's 201 transmitting and receiving the I/O request from test vector 303a, and raising operability and observation nature using general-purpose GUI functions, such as Tcl/Tk.

[0043] Next, the logic emulation system 500·by which the logic verification approach which is the gestalt of operation of the second of this invention is enforced is explained with reference to drawing 4 . By the logic emulation system 500 of drawing 4 , an exclusive information processor etc. is connected instead of logic emulator equipment 101, and the technique of performing logic verification of the verification logical chip 508 is explained. As a configuration, the information processor 301 (A) by which LAN connection was made is the same as the gestalt of the first operation, and the same is said of the test vector 303. Moreover, the gestalt of this second operation explains an information processor 501 (C) as a personal computer which considers as an example, for example, operates by the Windows system OS which is general-purpose OS for personal computers. An information processor 501 (C) consists of the Tcl/Tk interpreter 503, a processing control program 201, a driver control program 601, and a device driver 505.

[0044] And the exclusive information processor 502 connected to an information processor C by parallel I/O interface 506 consists of a control device 507, a verification logical chip 508, and RAM509. The verification logical chip 508 here manufactures logical structure model 307for verification a (logic 307 for verification) in the gestalt of the first operation as an actual chip. And test vector 303a (test vector 303) used with the gestalt of the first operation is set to the test vector storage area 106 of RAM509 as it is.

[0045] A device driver 505 is a controllable device driver about parallel I/O interface 506 in the device driver of the Windows system OS. And when the driver control program 601 for controlling this device driver 505 has an interface with the connecting plug interface 207 of the processing control program 201, the processing control program 201 and a device driver 505 are connected, and the processing control program 201 makes the whole system controllable. And the exclusive information processor 502 is controlled by controlling a control unit 507 via a device driver.

[0046] Moreover, the Tcl/Tk interpreter 503 is an interpreter of Tcl/Tk of the Windows system OS version, and, as for the processing control program 201, also in the Windows system OS version, the thing of the UNIX system OS version of the gestalt of the first operation can operate as it is.

[0047] Therefore, the verification purpose of the gestalt of this second operation is verifying the logic quality of a logical chip using the test vector 303 and the processing control program 201 which were used by the logic emulation, when the logical chip carried in the system is manufactured. That is, it is performing logic quality verification of a logical chip simple substance before system system verification.

[0048] Next, the outline of the driver control program 601 is shown in drawing 5 . The driver control program 601 consists of a control section 602, the processing control program interface section 603, a device driver control section 604, and a log data extraction control section 605. A control section 602 controls the whole driver control program 601, and the processing control program interface section 603 controls control lead of RAM access from the processing control program 201, or the exclusive information processor 502. The device driver control section 604 has an interface with a device driver 505, and controls parallel I/O interface 506 via a device driver. The log data extraction control section 605 extracts log data acquirable [with the driver control program 601], and has the function outputted or saved as log information 504.

[0049] Next, the concrete processing flow of the gestalt of the second operation is shown and explained to drawing 6 . By drawing 6 , the exclusive information processor 502 explains [the test control program 305 in the middle of of operation] a processing flow paying attention to the part of this invention when generating a message output demand and a command input demand. First, the processing stage in drawing 6 is classified into the stage of an operator 701, the processing control program 201, the driver control program 601, and the test control program 305, and expresses the whole processing flow.
[0050] The above-mentioned verification logical chip 508 is set in the exclusive information processor 502, test vector 303a is set to the test vector storage area 106 of RAM509, and when it is in the waiting state waiting for initiation directions of operation, an operator 701 performs verification initiation directions (step 702). Next, the processing control program 201 performs initiation directions of operation to the driver control program 601 (step 703), and the driver control program 601 operates the exclusive information processor 502 (step 704). If equipment operates, the test control program 305 will start actuation (step 705). Moreover, the processing control program 201 starts the monitor of interface information, after performing step 703 (step 706). Under the monitor of the interface information 306, for polling access of RAM509, the driver control program 601 always performs RAM access, and is performing RAM read-out (step 707). When it is in these conditions, the test control program 305 will set a message and an event to interface information, if the output request of a message and a command input demand occur (step 708) (step 709). Next, the processing control program 201 which is supervising interface information 306 detects this event as a demand (step 710), and acquires the interface information 306 (step 711). Data conversion of the acquired data is carried out (step 712), and they are displayed on a window as a message (step 713). After a display, an operator 701 performs a key input and a window operation (step 715) to a command input demand (step 714).
[0051] Next, the processing control program 201 of an input waiting state acquires (step 716) and the inputted key input (step 717), performs data conversion (step 712), and transmits it to (step 718) and the test control program 305 by writing in RAM509 as interface information 306 (step 719). The processing control program 201 goes into the executive state of the interface information 306 again after a transfer (step 706). If it is working even after the test control program 305 advances the demand of said step 708 (step 720), and an input event is detected from the transmitted interface information 306 (step 721), from the interface information 306, an input command will be acquired (step 722) and actuation to the acquired command will be performed (step 723). Such a series of actuation is performed and logic verification of the verification logical chip 508 is performed interactively.
[0052] Moreover, it is usable as it is in the test vector 303 and the processing control program 201 which were common in the gestalt of the first operation, and it is possible to perform simple substance verification of the logic emulation using the logical structure model 105 for verification and the real chip of verification logical chip 508 grade in the same environment, and the logic verification which cohered until it resulted [from a logical model] in a real chip is attained.
[0053] That is, by the ability of software and a test vector common to the logic verification process by the logic emulation using logic emulator equipment 101, and the logic verification process by the real chip of verification logical chip 508 grade to be used, the effort which overlapped [prepare / according to each process / software or a test vector] can be mitigated, and efficient logic verification is attained.
[0054] Next, the logic emulation system 800 by which the logic verification approach which is the gestalt of operation of the third of this invention is enforced is shown in drawing 7 . In the logic emulation system 800 of drawing 7 , a logic simulator is added to the gestalt of operation of the first of drawing 1 , and the case where they are the logic emulator with which the logic verification technique differs from logic verification level, and the logic verification method with which a logic simulator is intermingled is illustrated.
[0055] The case where make logic actuation of a microprocessor etc. specifically as a gestalt of this third operation perform by the logic simulator 802, and logic verification of both sides in the actuation with which both cooperated is performed with logic emulator equipment 101 before finishing setting up the system which is mounting logic of the I/O-hardware-control device used

by the system containing this microprocessor, and used both real chips can be considered.
[0056] The logic simulator 802 in the gestalt of this third operation is a functional level instruction simulator, and explains a logic simulator 802 as microinstruction actuation. On an information processor 801 (D), the logic emulator control program 109, the processing control program 201, and a logic simulator 802 are started. Among these three programs, a logic simulator 802 is connected by the connecting plug interface 207 of the processing control program 201, and the interprocess communication control section 203 performs interprocess communication. Therefore, the processing control program 201 has generalized and controlled the whole system.
[0057] As a procedure of logic verification, logic emulator equipment 101 is operated in the way of the gestalt of the first operation, and it considers as the condition which can be operated. Next, the processing control program 201 starts a logic simulator 802, and the test vector (test instruction train) 806 given to a logic simulator 802 is set to the RAM model 805. In addition, the logic simulator 802 who takes up here explains as what considers as a common functional level instruction logic simulator, and uses the processing control section 803, a logical model 804, and the RAM model 805 as a component.
[0058] Next, if simulation of the test instruction train of the test vector 806 set by the logic simulator 802 is carried out one by one, when carrying out simulation of the instruction train with special semantics and the special-instruction train is accompanied by microinstruction actuation, a logic simulator 802 sets the contents of the current RAM model 805 to the interface information 306, and demands microinstruction actuation from logic emulator equipment 101. This demand is told to the processing control program 201 by processing control-section 803 course, and transmits the set interface information to the interface information 306 on logic emulator equipment 101. A logic simulator 802 resumes the simulation of a test instruction train succeedingly, after advancing a demand. Moreover, after transmitting interface information, the processing control program 201 operates logic emulator equipment 101, and the logic simulator 802 and logic emulator equipment 101 start actuation to asynchronous completely at this time. Next, if only a fixed cycle performs an emulation, microinstruction actuation will be completed and logic emulator equipment 101 will interrupt actuation for the same procedure as the gestalt of the first operation. Although transmitted to a logic simulator 802 by making a suspended state into interface information at this time, a synchronization / asynchronous-control section 217 takes a synchronization with the logic simulator 802 who is operating to asynchronous.
[0059] Since this synchronization / asynchronous-control section 217 have expected the logic emulation finish time beforehand by the logic simulator 802 side when a logic simulator 802 advances a microinstruction operational request, it controls the case where a logic simulator 802 will perform queuing if only the number of fixed instructions carries out simulation of the test instruction train, and the case where it reports to a logic simulator 802 as interrupt processing when simulation has not completed only the number of fixed instructions.
[0060] The processing control section 803 manages the reported emulation completion report, and the simulation of a test instruction train is controlled. It carries out by repeating processing of these single strings, and logic verification is performed. Thus, by the logic verification method by which the logic simulator 802 and logic emulator equipment 101 are intermingled, transmitting interface information mutually, suiting and taking the adjustment of a verification condition, in the middle of verification, it operates to asynchronous completely and efficient logic verification is performed. Moreover, if it is possible to unify a connection interface since it connects using the connecting plug interface 207 when connecting a logic simulator 802, it is possible to deal with a logic verification means by which can connect no matter it may be what logic verification technique, and plurality differs further, collectively.
[0061] The false logical model 304 built into the logical structure model 105 for verification as the gestalt of the first operation explained as mentioned above, By performing transfer of the test control program 305 built into test vector 303a, and these and information It becomes establishable [the interactive logic verification method which was excellent in incorporating the processing control program 201 which controls a logic emulation at the high speed which made the most of the rapidity of logic emulator equipment 101, and operability and observation

nature] from the exterior.
[0062] As illustrated in the gestalt of the second operation, the processing control program 201 moreover, for example, by being described by general purpose languages, such as Tcl/Tk independent of execution environments, such as OS The test vector 303 and the processing control program 201 which were used with the gestalt of the first operation are used as it is. It is possible to be able to build the environment in which logic verification of the real chip of verification logical chip 508 grade is possible, and for the logic verification which cohered until it resulted [from a logical model] in a real chip to be attained, and to perform logic verification efficiently.
[0063] Moreover, as illustrated in the gestalt of the third operation, the logic verification which took the adjustment of asynchronous operation by connect the logic verification technique in_which of verification level differ, like a logic simulator 802 and logic emulator equipment 101 grade, and transmit interface information mutually be possible, for example, the logic verification verification and a microprocessor cohered as the whole equipment of large-scale logic, such as the whole system which consist of I/O hardware control devices of the peripheral device etc., be possible.
[0064] Although invention made by this invention person above was concretely explained based on the gestalt of operation, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the gestalt of said operation, and does not deviate from the summary.
[0065]
[Effect of the Invention] According to the logic verification approach of this invention, the effectiveness that system-logic verification by the logic emulation in the whole logical chip can be performed in a short time efficiently is acquired.
[0066] Moreover, a man machine interface is enriched and the observation nature of the internal state in a logic emulation, operability, and the effectiveness that test ease can be raised further are acquired.
[0067] Moreover, the effectiveness that the logic verification which cohered until it resulted [from a logical model] in a real chip is realizable is acquired.
[0068] Moreover, the man day and period which environmental construction of logic verification takes are shortened, and the effectiveness that the cost reduction in a logic verification process is realizable is acquired.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the conceptual diagram showing an example of the configuration of the information processing system with which the logic verification approach which is the gestalt of operation of the first of this invention is enforced.
[Drawing 2] It is the conceptual diagram having shown an example of the configuration of the software for realizing the logic verification approach of this invention.
[Drawing 3] It is the flow chart which shows an example of an operation of the logic verification approach which is the gestalt of operation of the first of this invention.
[Drawing 4] It is the conceptual diagram showing an example of the configuration of the information processing system with which the logic verification approach which is the gestalt of operation of the second of this invention is enforced.
[Drawing 5] It is the conceptual diagram having shown an example of the configuration of the software used by the logic verification approach which is the gestalt of operation of the second of this invention.
[Drawing 6] It is the flow chart which shows an example of an operation of the logic verification approach which is the gestalt of operation of the second of this invention.
[Drawing 7] It is the conceptual diagram having shown an example of the configuration of the software used by the logic verification approach which is the gestalt of operation of the third of this invention.
[Drawing 8] It is the conceptual diagram showing an example of the logic emulation structure of a system which is the reference technique of the logic verification approach of this invention.
[Description of Notations]
100 -- A logic emulation system, 101 -- Logic emulator equipment, 102 [-- The logical structure model storage area for verification,] -- A control device, 103 -- RAM, 104 -- Clock generation equipment, 105 106 -- A test vector storage area, 107 -- A control signal pin, 108 -- Information processor, 109 -- A logic emulator control program, 110 -- A control section, 111 -- Logic compiler, 112 -- The RAM access section, 113 -- A GUI control section, 113 -- Graphical user interface control section, 114 -- The logic for verification, 114a -- The logical structure model for verification, 201 -- Processing control program, 202 -- A GUI control section, 203 -- An interprocess communication control section, 204 -- Logic emulator control section, 205 -- A test vector control section, 206 -- The data-conversion section, 207 -- Connecting plug interface, 208 -- A trigger event control section, 209 -- A control section of operation, 210 -- RAM access section, 211 [-- Window control section,] -- A processing control section, 212 -- A display, 213 -- The input-control section, 214 215 -- A setting information control section, 216 -- A log data extraction control section, 217 -- A synchronization / asynchronous-control section, 300 -- A logic emulation system, 301 -- An information processor, 302 -- Information processor, 303 -- A test vector, 303a -- A test vector, 304 -- False logical model (2nd logical structure model), 305 -- A test control program, 306 -- Interface information, 307 -- Logic for verification, 307a -- The logical structure model for verification (1st logical structure model), 308 -- Log information, 500 -- A logic emulation system, 501 -- An information processor, 502 -- An exclusive information processor, 503 -- A Tcl/Tk interpreter, 504 -- Log information, 505 --

Device driver, 506 -- A parallel I/O interface, 507 -- A control device, 508 -- Verification logical chip (purpose logical unit), 509 -- RAM, 601 -- A driver control program, 602 -- Control section, 603 -- The processing control program interface section, 604 -- Device driver control section, 605 [-- A logic simulator, 803 / -- A processing control section, 804 / -- A logical model, 805 / -- A RAM model, 806 / -- Test vector.] -- A log data extraction control section, 800 -- A logic emulation system, 801 -- An information processor, 802

[Translation done.]